Box 1:
Internal Reports Vol I
 operation Performance of 10-Digit Shifting Register Experimental Model, 1949
 The Marginal Checking System, 1949
 Diode Pulse Circuit for Shift Register, 1949
 First 10-Digit Arithmetic Unit for Test Purposes, 1949
 Speed Tests on Arithmetic Units, 1949
 The Relay Circuits for the Input-Output Equipment, 1949
 Tube and Resistor Tolerances for Shift Registers, 1949
 Measurements of Magnetic Field Strengths in the Physical Plant Service Building, 1950
 Resolver Tube Test Conditions, 1950
 Digit Resolver Tube Test Conditions, 1950
 Adder Tube Test Characteristics, 1950
 Reversible Magnetic Transformations in “Deltamax” Toroidal Cores, 1950
 Selectron Operating Test, 1950
 Construction and Tests of the Low-Speed Input-Output Equipment, 1950
 Forty Digit Arithmetic Unit, 1950
 Arithmetic Unit Tests, 1950
 Further Tests of the Low-Speed Input-Output Equipment, 1950
 A Storage System for an Electronic Digital Computer, 1950
 Preliminary Design of an Arithmetic Unit for Use with a Self-Checking Binary Parallel Digital
 Computer, 1950
 A Testing Apparatus for a Williams Tube Storage System, 1950
 A Circuit for Studying the Secondary Emission Characteristics of Cathode Ray Tube Phosphors,
 1950
 Screen Imperfections in Type 3KP1 Cathode Ray Tubes, 1950
 A Space-Saving Sorting Routine, 1950
 A Test Problem, 1950
 IBM Card Input-Output Conversion Routines for the ORDVAC, 1951
 Preliminary Considerations on a Magnetic Drum Controlled Computer, 1951
 Restoring and Non-Restoring Division, 1951
 Results of Reading, Writing and Read-Around Tests, 1951
 Phosphor Contamination II, 1951
 A Comparison of Read-Around-Ratio Tests in Williams IV and Williams II, 1951
 The ORDVAC, 1951
 A Routine for Calculating the Eigenvalues and Eigenvectors of a Symmetric Matrix, 1952
 Program Organization for the University of Illinois Digital Computer, 1952
 Selection Tests on 3KP1 Type Cathode Ray Tubes for a Williams Memory, 1952
 ORDVAC Order Code, 1952
 Order Code for University of Illinois Electronic Digital Computer, 1952

Internal Reports Vol II
Error Detection and Correction in Binary Parallel Digital Computers, 1952
Revised Order Code for the University of Illinois Digital Computer, 1952  
How to Calculate the Read-Around Requirements of a Code, 1952  
Operation Times of the Illinois Computer, 1952  
Comparison of Four IBM Tubes with 3KP1 Tubes for Williams Memory Use, 1952  
Operation Times of ILLIAC, 1953  
The Calculation of 60,000 Digits of e by the ILLIAC, 1953  
Controls of the ILLIAC and Input and Output Equipment, 1953  
Improvement of the ILLIAC Memory, 1953  
Metric Properties of Boolean Algebra and their Application to Switching Circuits, 1953  
Results of Tests on 25 Bureau of Ships-RCA Developmental Williams Memory Tubes + Type C-73376B, 1953  
DC Tolerance Analysis of a High Speed Transistor Flip-Flop, 1953  
ILLIAC Order Code, 1953  
The Deutron Problem with Tensor Forces, 1953  
Minimization of v Polynomials Subject to Subsidiary Conditions, 1953  
Static Magnetic Memory, 1953  
Operational Results Using C73621 Cathode Ray Tubes as Storage Tubes  
A Dynamic Magnetic Core Memory, 1953  
Reorganization of ILLIAC Library, 1954  
Modification of Teletype Equipment, 1954  
Some Theorems on the Metric Properties of Boolean Algebra, 1954

Internal Reports Vol III  
An Upper Bound for the Number of Certain Error Correcting Codes, 1954  
A Bound on the Error in a General Quadrature Formula with Equidistant Ordinates, 1954  
On the Convergence Rate of an Iterative Process, 1954  
Operating Instructions for Protoelectric Paper Tape Comparer, 1955  
A Brief Description of the Routines in the ILLIAC Active Program Library, 1955  
Fundamentals of Junction Transistor Physics, 1955  
Some Direct-Coupled Computer Circuits Utilizing NPN and PNP Transistors in Combination, 1955  
Theory of Asynchronous Circuits, 1955  
Coaxial Cable Memory, 1957  
Organization of a Very High-Speed Computer, 1959  
A Study of Redundant Number Representations for Parallel Digital Computers, 1960